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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/564,473	01/13/2006	Masaki Murase	SON-3058	9263

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EXAMINER	
SITTA, GRANT	

ART UNIT	PAPER NUMBER
2629	

MAIL DATE	DELIVERY MODE
03/10/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/564,473	MURASE ET AL.	
	Examiner	Art Unit	
	GRANT D. SITTA	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 January 2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/13/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1-3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claim 6 is objected to because of the following informalities: "(CGS)" needs to be fully written out one time. Appropriate correction is required. Examiner suggests "…continuous grain silicon (CGS)"

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Kitagishi et al (5,736,972) hereinafter, Kitagishi.

5. In regards to claim 1, Kitagishi delay time correction circuit (fig. 1 (7)), characterized by inserting, for a data processing circuit for processing input data having a quiescent period (col. 8, lines 42-67) during which the input data is held at a constant logical level for a constant period at a constant cycle (col. 5, lines 38-59), dummy data having a logical level opposite to the constant logical level into the input data at a predetermined timing during the quiescent period (fig. 2 dummy data and col. 8, lines 42-67).

6. In regard to claim 2, Kitagishi teaches data processing circuit for processing input data having a quiescent period (col. 8, lines 42-67) during which the input data is held at a constant logical level for a constant period at a constant cycl (fig. 2 dummy data and col. 8, lines 42-67)e, characterized by inserting dummy data having a logical level opposite to the constant logical level into the input data at a predetermined timing during the quiescent period (fig. 2 dummy data and col. 8, lines 42-67).

7. In regards to claim 3, Kitagishi teaches the data processing circuit according to claim 2, characterized in that: the input data is video data (abstract); and the quiescent period is a horizontal blanking period or a vertical blanking period (col. 8, lines 20-25).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and

the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagishi in view of Yun et al (7,259,739) hereinafter, Yun.

11. In regards to claim 4, Kitagishi discloses the limitations of a flat display device comprising (abstract LCD): a display section having pixels arranged in a matrix form (col. 1, lines 42-62) characterized in that a gradation data is processed by inserting dummy data having a logical level opposite to a logical level during a horizontal blanking period into the gradation data at a predetermined timing during the horizontal blanking period of the gradation data.

Kitagishi differs from the claimed invention in that Kitagishi does not expressly disclose a vertical driving circuit for sequentially selecting pixels of the display section through gate lines); and a horizontal driving circuit for converting gradation data indicative of gradations of the pixels into analog signals by sequentially sampling the gradation data, and driving the pixels selected through the gate lines by driving signal lines of the display section by the analog signals,

However, Yun teaches a system and method for a vertical driving circuit (fig. 6 (14)) for sequentially selecting pixels of the display section through gate lines (col. 18, lines 57-67); and a horizontal driving circuit for converting gradation data indicative of gradations of the pixels (fig. 6 (16)) into analog signals by sequentially sampling the gradation data (col. 18, lines 57-67), and driving the pixels selected through the gate lines by driving signal lines of the display section by the analog signals (col. 9-10, lines 10- 55 of Yun).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Kitagishi to include the use of a vertical driving circuit for sequentially selecting pixels of the display section through gate lines; and a horizontal driving circuit for converting gradation data indicative of gradations of the pixels into analog signals by sequentially sampling the gradation data, and driving the pixels selected through the gate lines by driving signal lines of the display section by the analog signals as taught by Yun in order to provide a method of driving a display that enhances display quality as stated in (col. 3, lines 40-67 of Yun).

12. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kitagishi and Yun, in view of Ochiai et. al (US 6,897,909) hereinafter, Ochiai.

13. In regards to claim 5, Kitagishi and Yun differ from the claimed invention in that Kitagishi does not disclose characterized in that an active devices for processing the gradation data is formed by low-temperature polysilicon.

However, Ochiai teaches a system and method for characterized in that an active devices for processing the gradation data is formed by low-temperature polysilicon. (col. 11, lines 13-43 of Ochiai).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Kitiaishi and Yun to include the use of an active devices for processing the gradation data is formed by low-temperature polysilicon as taught by Ochiai in order to because they are faster than amorphous silicon TFTs. Now you can place the drivers and shift registers on the same substrate as the LCD cells. This approach allows for very high resolution displays.

14. In regards to claim 6, Kitagishi and Yun differ from the claimed invention in that Kitagishi and Yun do not disclose an active devices for processing the gradation data is formed by CGS.

However, Ochiai teaches a system and method for an active devices for processing the gradation data is formed by CGS (col. 23, lines 39-52).

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to modify Kitagishi and Yun to include the use of an active devices for processing the gradation data is formed by CGS as taught by Ochiai in order to smaller

sized TFTs which save space and enable more light to pass through to the viewe for better picture quality.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to GRANT D. SITTA whose telephone number is (571)270-1542. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Sumati Lefkowitz/
Supervisory Patent Examiner, Art Unit 2629

/Grant D Sitta/
Examiner, Art Unit 2629
March 3, 2009